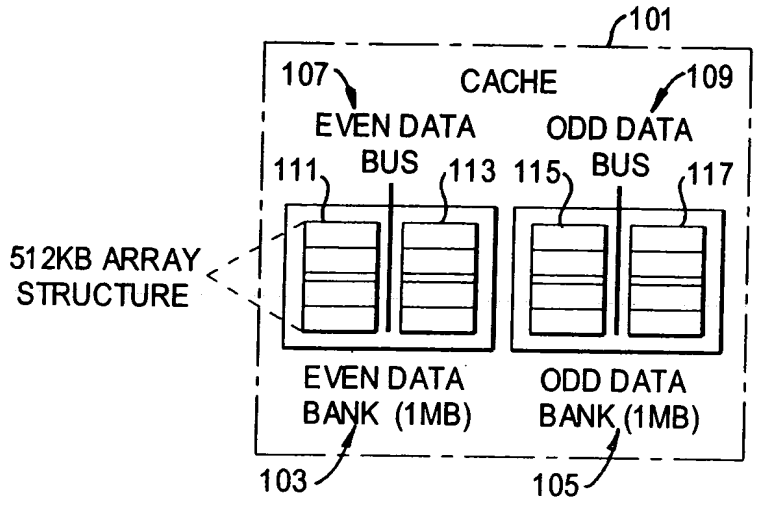

101
107
CACHE
109
EVEN DATA BUS
ODD DATA BUS
111
113
115
117
512KB ARRAY STRUCTURE
EVEN DATA BANK (1MB)
ODD DATA BANK (1MB)
103
105

FIG. 1

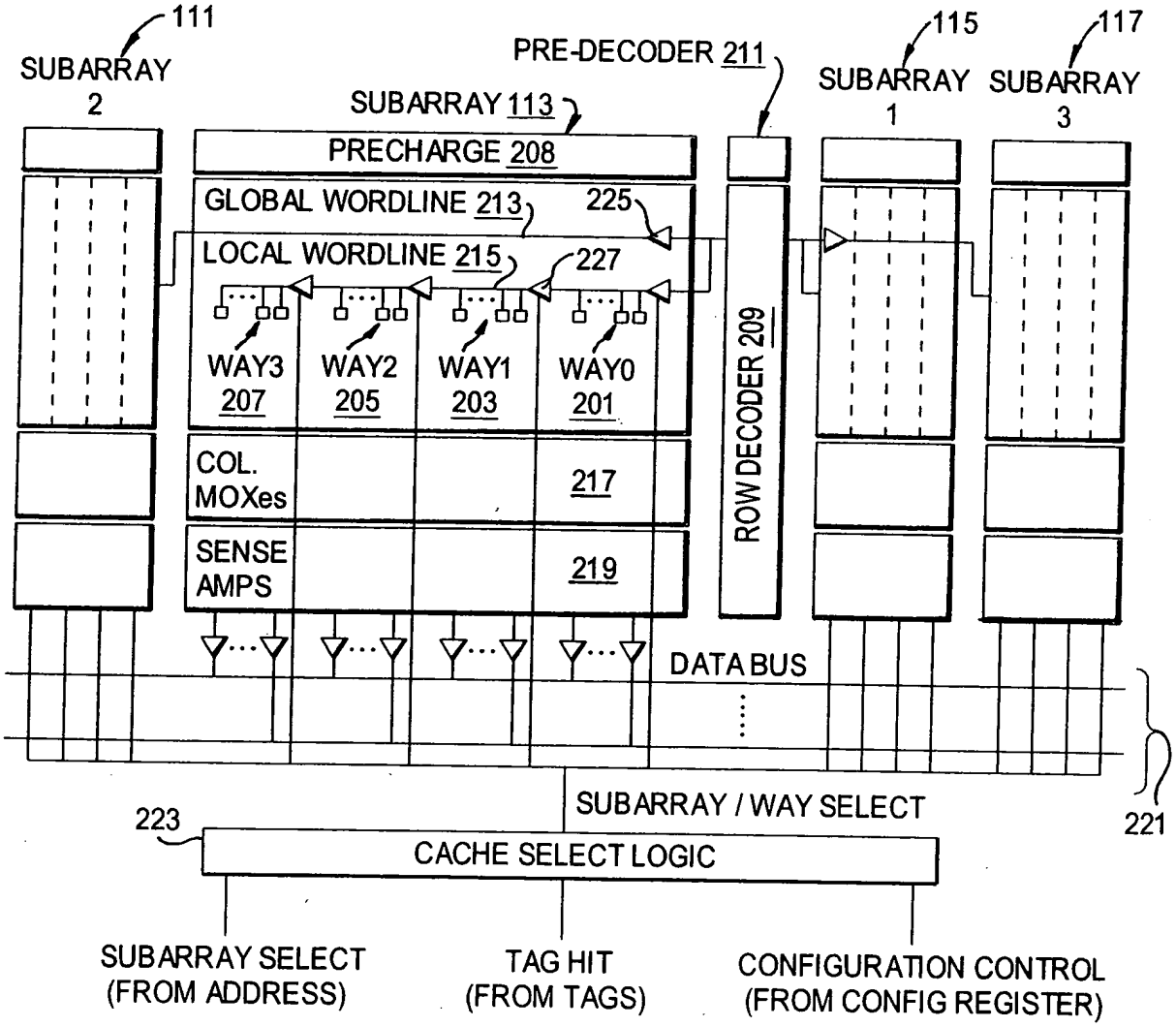

111
SUBARRAY 2
PRE-DECODER 211
115
117
SUBARRAY 1
SUBARRAY 3
SUBARRAY 113
PRECHARGE 208
GLOBAL WORDLINE 213
225
LOCAL WORDLINE 215
227
WAY3 207
WAY2 205
WAY1 203
WAY0 201
ROW DECODER 209
COL. MOXes
217
SENSE AMPS
219
DATA BUS
221
SUBARRAY / WAY SELECT
223
CACHE SELECT LOGIC
SUBARRAY SELECT (FROM ADDRESS)
TAG HIT (FROM TAGS)
CONFIGURATION CONTROL (FROM CONFIG REGISTER)

FIG. 2

SUBARRAY / WAY ALLOCATION (L1 OR L2)

CACHE CONFIGURATION	L1 SIZE	L1 ASSOC	L1 ACC TIME	SUBARRAY 2				SUBARRAY 0				SUBARRAY 1				SUBARRAY 3			
				W3	W2	W1	W0	W3	W2	W1	W0	W0	W1	W2	W3	W0	W1	W2	W3
256-1	256KB	1 WAY	2.0	L2	L2	L2	L2	L2	L2	L2	L1	L1	L2	L2	L2	L2	L2	L2	L2
512-2	512KB	2 WAY	2.5	L2	L2	L2	L2	L2	L2	L1	L1	L1	L1	L2	L2	L2	L2	L2	L2
768-3	768KB	3 WAY	2.5	L2	L2	L2	L2	L2	L1	L1	L1	L1	L1	L1	L2	L2	L2	L2	L2
1024-4	1024KB	4 WAY	3.0	L2	L2	L2	L2	L1	L1	L1	L1	L1	L1	L1	L1	L2	L2	L2	L2
512-1	512KB	1 WAY	3.0	L2	L2	L2	L1	L2	L2	L2	L1	L1	L2	L2	L2	L1	L2	L2	L2
1024-2	1024KB	2 WAY	3.5	L2	L2	L1	L1	L2	L2	L1	L1	L1	L1	L2	L2	L1	L1	L2	L2
1536-3	1536KB	3 WAY	4.0	L2	L1	L1	L1	L2	L1	L1	L1	L1	L1	L1	L2	L1	L1	L1	L2
2048-4	2048KB	4 WAY	4.5	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1	L1

FIG. 3

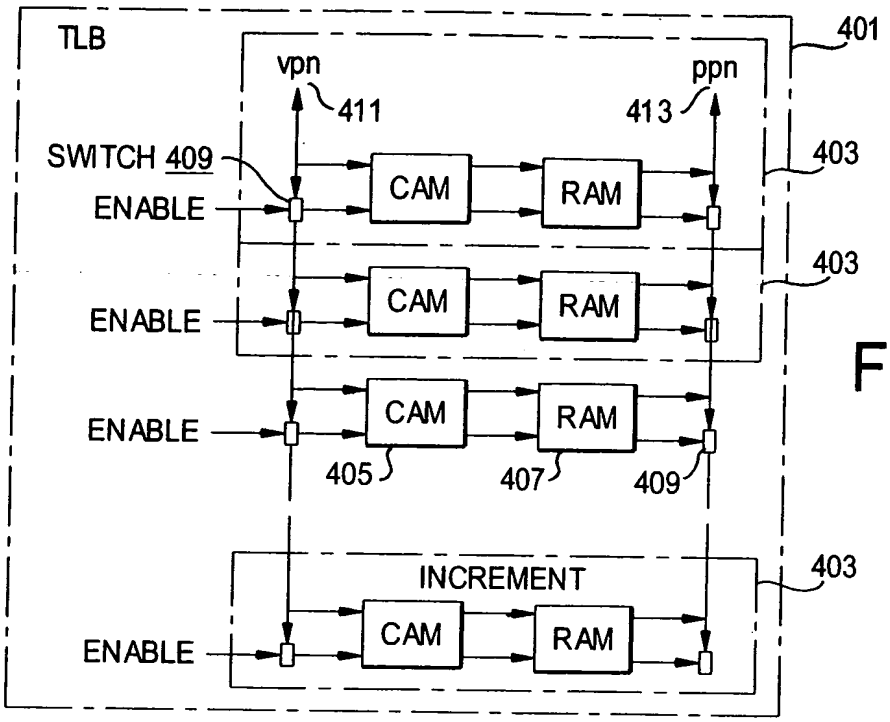
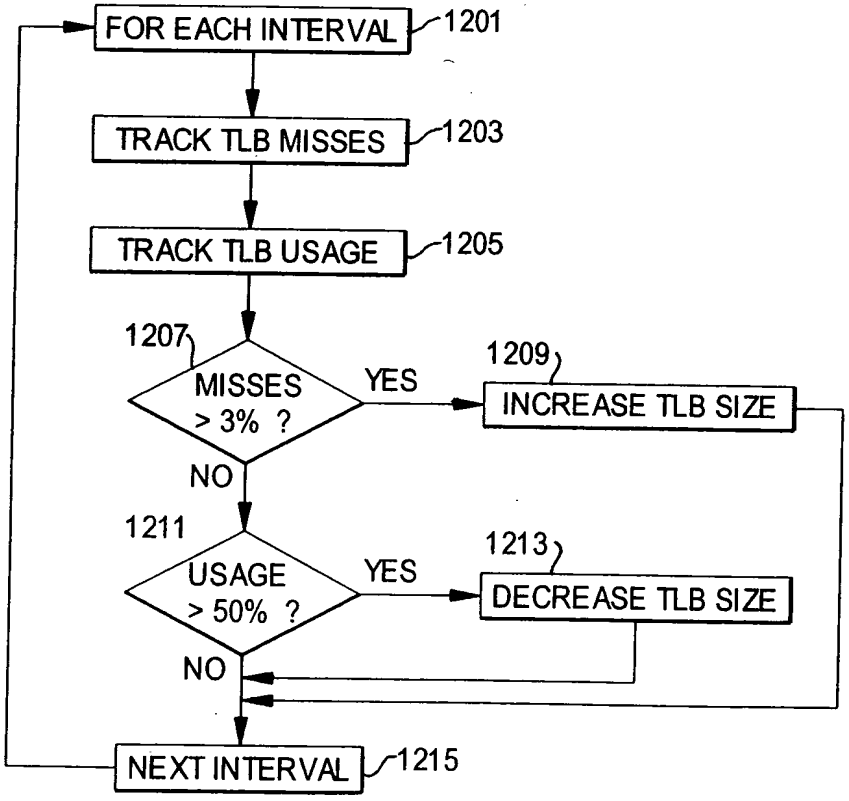

TLB
401
vpn
411
ppn
413
SWITCH 409
ENABLE
CAM
RAM
403
ENABLE
CAM
RAM
403
ENABLE
CAM
RAM
405
407
409
INCREMENT
403
ENABLE
CAM
RAM

FIG. 4

FIG. 12


FOR EACH INTERVAL
1201
TRACK TLB MISSES
1203
TRACK TLB USAGE
1205
1207
MISSES > 3% ?
YES
1209
INCREASE TLB SIZE
NO
1211
USAGE > 50% ?
YES
1213
DECREASE TLB SIZE
NO
NEXT INTERVAL
1215

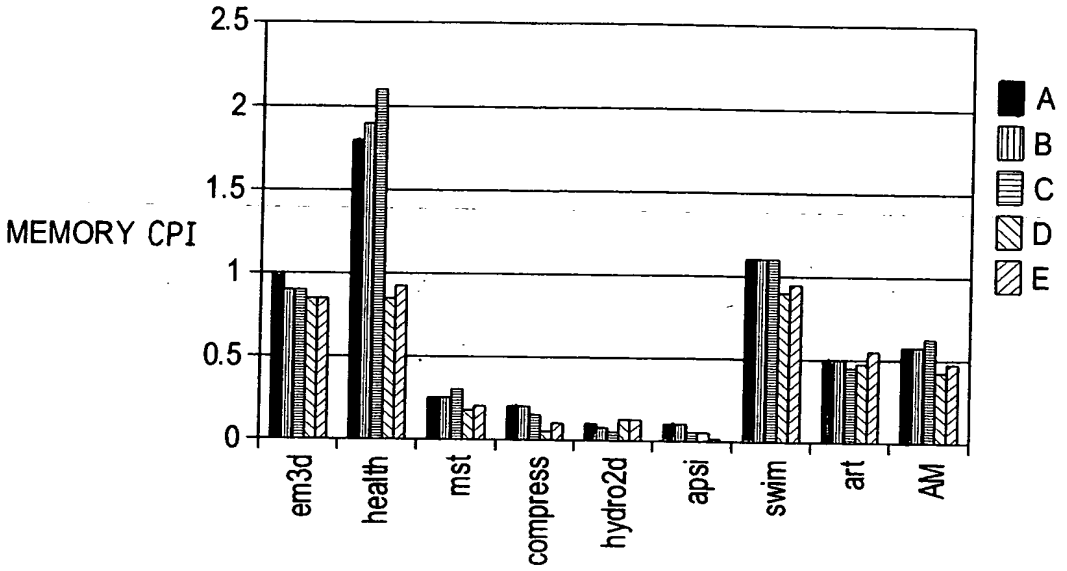

MEMORY CPI
2.5
2
1.5
1
0.5
0
em3d
health
mst
compress
hydro2d
apsi
swim
art
AM
A
B
C
D
E

FIG. 5

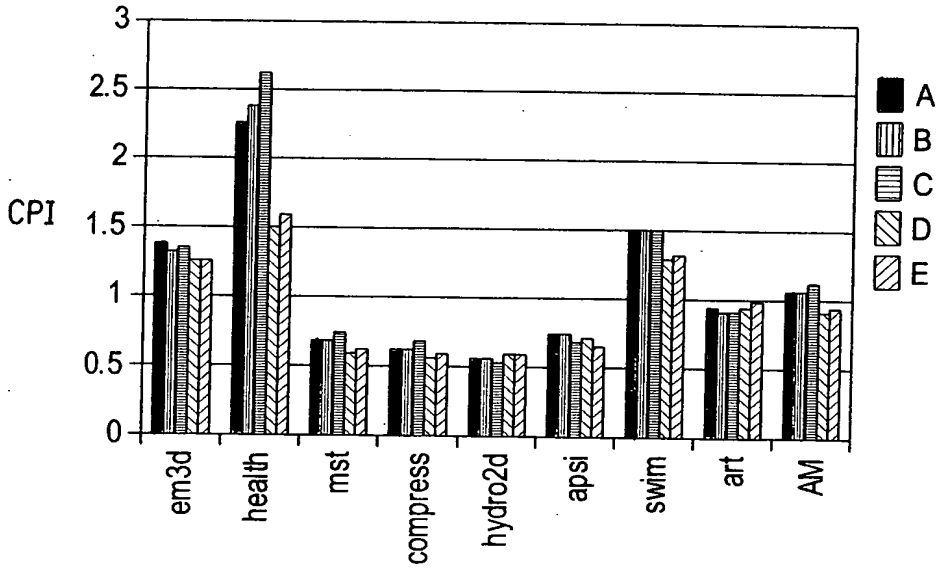

CPI
3
2.5
2
1.5
1
0.5
0
em3d
health
mst
compress
hydro2d
apsi
swim
art
AM
A
B
C
D
E

FIG. 6

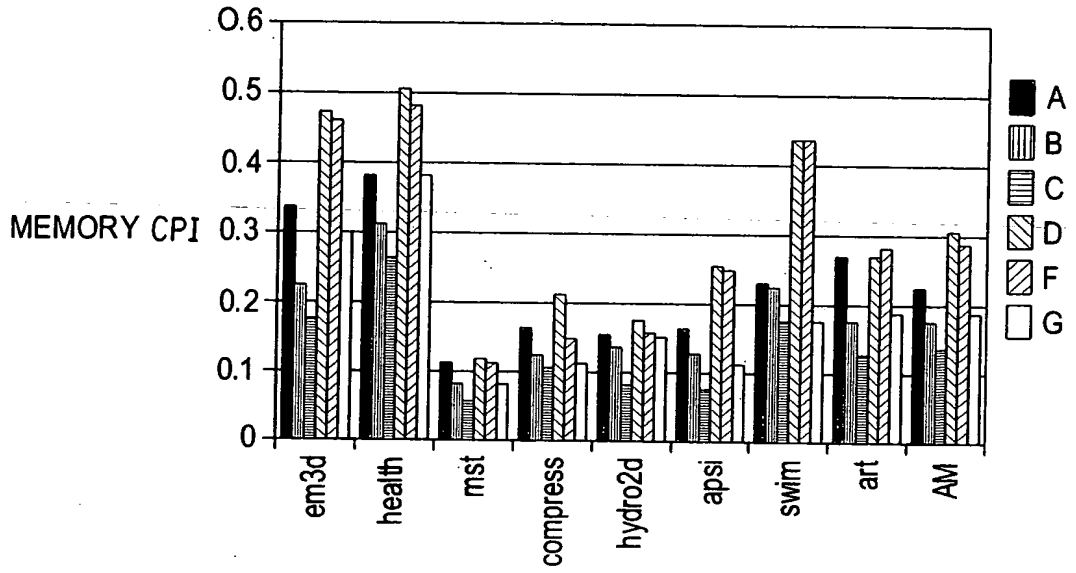

MEMORY CPI
0.6
0.5
0.4
0.3
0.2
0.1
0
em3d
health
mst
compress
hydro2d
apsi
swim
art
AM
A
B
C
D
F
G

FIG. 7

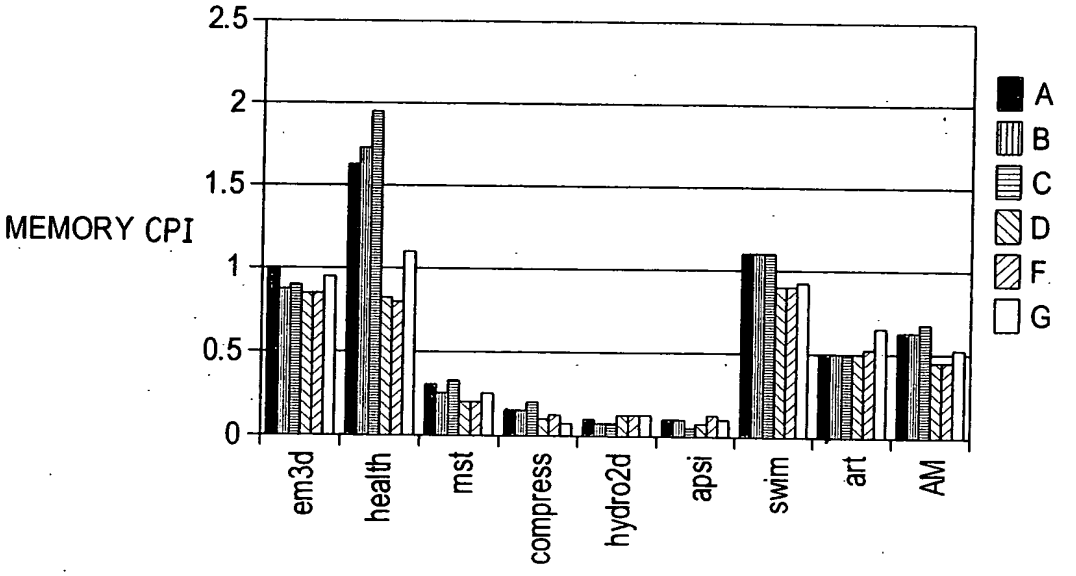

MEMORY CPI
2.5
2
1.5
1
0.5
0
em3d
health
mst
compress
hydro2d
apsi
swim
art
AM
A
B
C
D
F
G

FIG. 8

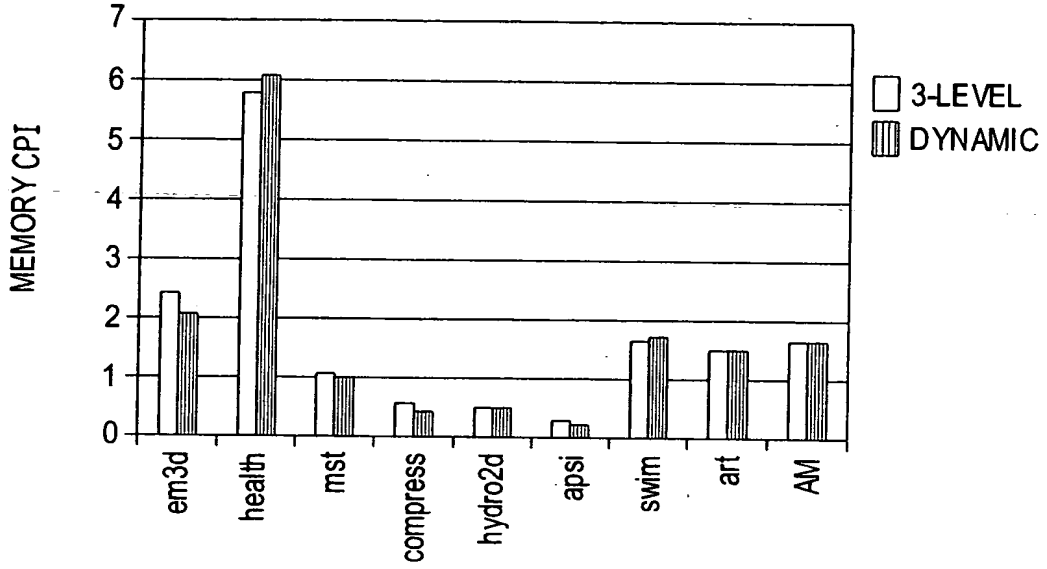

MEMORY CPI
7
6
5
4
3
2
1
0
em3d
health
mst
compress
hydro2d
apsi
swim
art
AM
3-LEVEL
DYNAMIC

FIG. 9

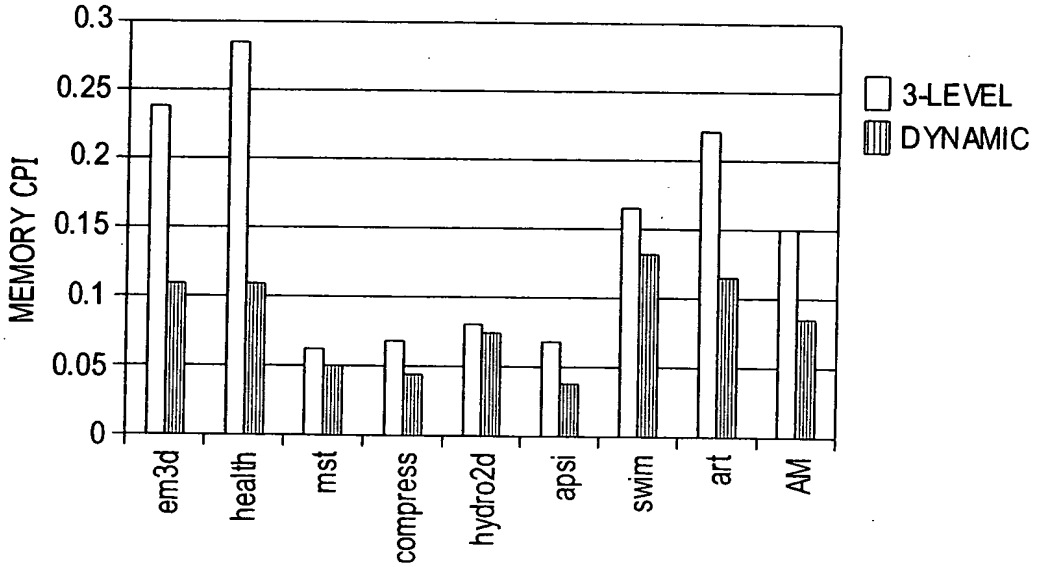

MEMORY CPI
0.3
0.25
0.2
0.15
0.1
0.05
0
em3d
health
mst
compress
hydro2d
apsi
swim
art
AM
3-LEVEL
DYNAMIC

FIG. 10

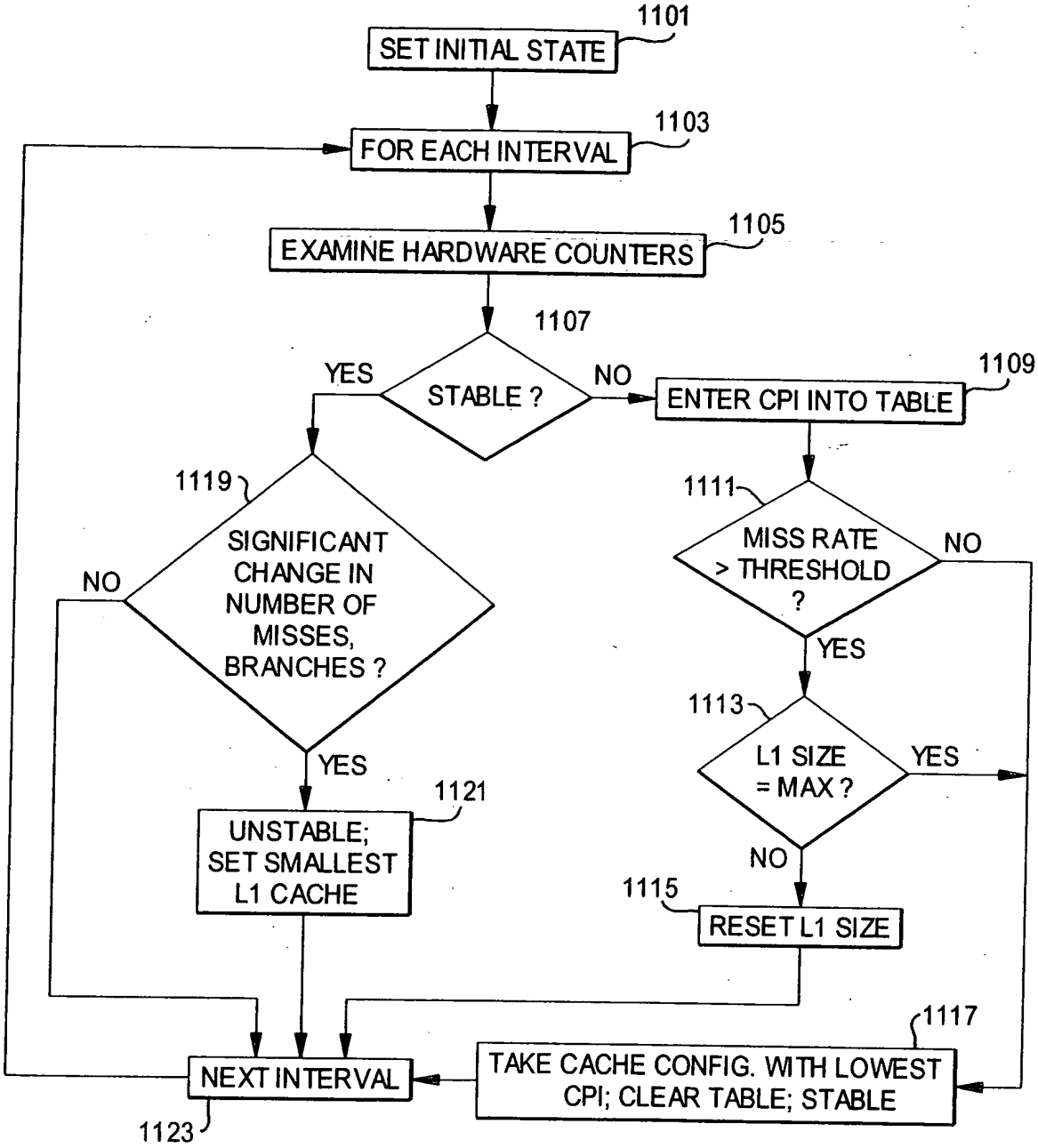

1101
SET INITIAL STATE
1103
FOR EACH INTERVAL
1105
EXAMINE HARDWARE COUNTERS
1107
STABLE ?
YES
NO
1109
ENTER CPI INTO TABLE
1111
MISS RATE > THRESHOLD ?
NO
YES
1113
L1 SIZE = MAX ?
YES
NO
1115
RESET L1 SIZE
1117
TAKE CACHE CONFIG. WITH LOWEST CPI; CLEAR TABLE; STABLE
1119
SIGNIFICANT CHANGE IN NUMBER OF MISSES, BRANCHES ?
NO
YES
1121
UNSTABLE; SET SMALLEST L1 CACHE
NEXT INTERVAL
1123

FIG. 11